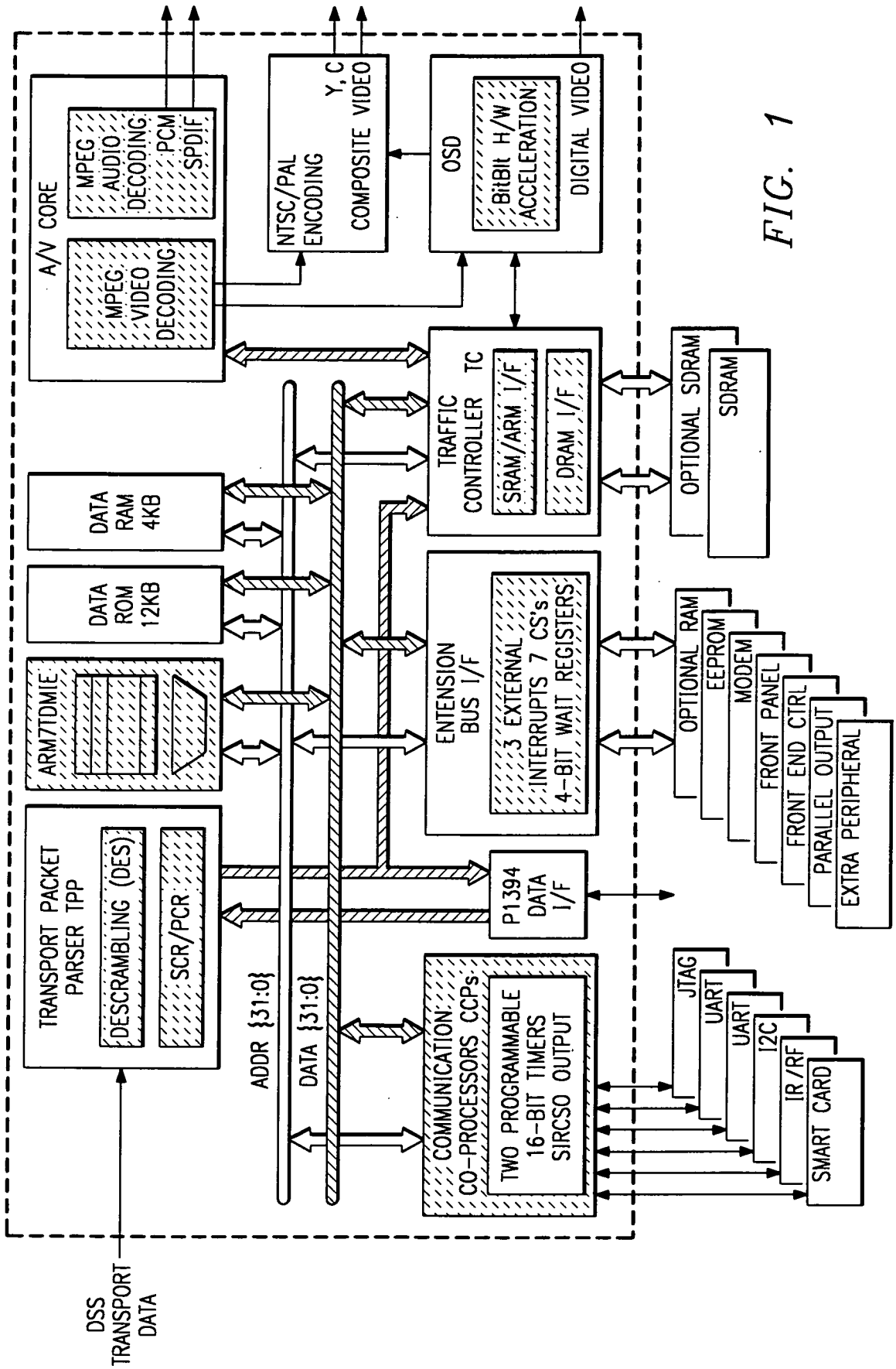

A/V CORE
MPEG AUDIO DECODING
PCM
SPDIF
MPEG VIDEO DECODING
NTSC/PAL ENCODING
Y, C
COMPOSITE VIDEO
OSD
BitBlt H/W ACCELERATION
DIGITAL VIDEO
TRAFFIC CONTROLLER TC
SRAM/ARM I/F
DRAM I/F
OPTIONAL SDRAM
SDRAM
DATA RAM 4KB
DATA ROM 12KB
ARM7TDMIE
ENTENSION BUS I/F
3 EXTERNAL INTERRUPTS 7 CS's
4-BIT WAIT REGISTERS
OPTIONAL RAM
EEPROM
MODEM
FRONT PANEL
FRONT END CTRL
PARALLEL OUTPUT
EXTRA PERIPHERAL
TRANSPORT PACKET PARSER TPP
DESCRAMBLING (DES)
SCR/PCR
P1394 DATA I/F
ADDR {31:0}
DATA {31:0}
COMMUNICATION CO-PROCESSORS CCPs
TWO PROGRAMMABLE 16-BIT TIMERS
SIRCSO OUTPUT
JTAG
UART
UART
I2C
IR/RF
SMART CARD
DSS TRANSPORT DATA

FIG. 1

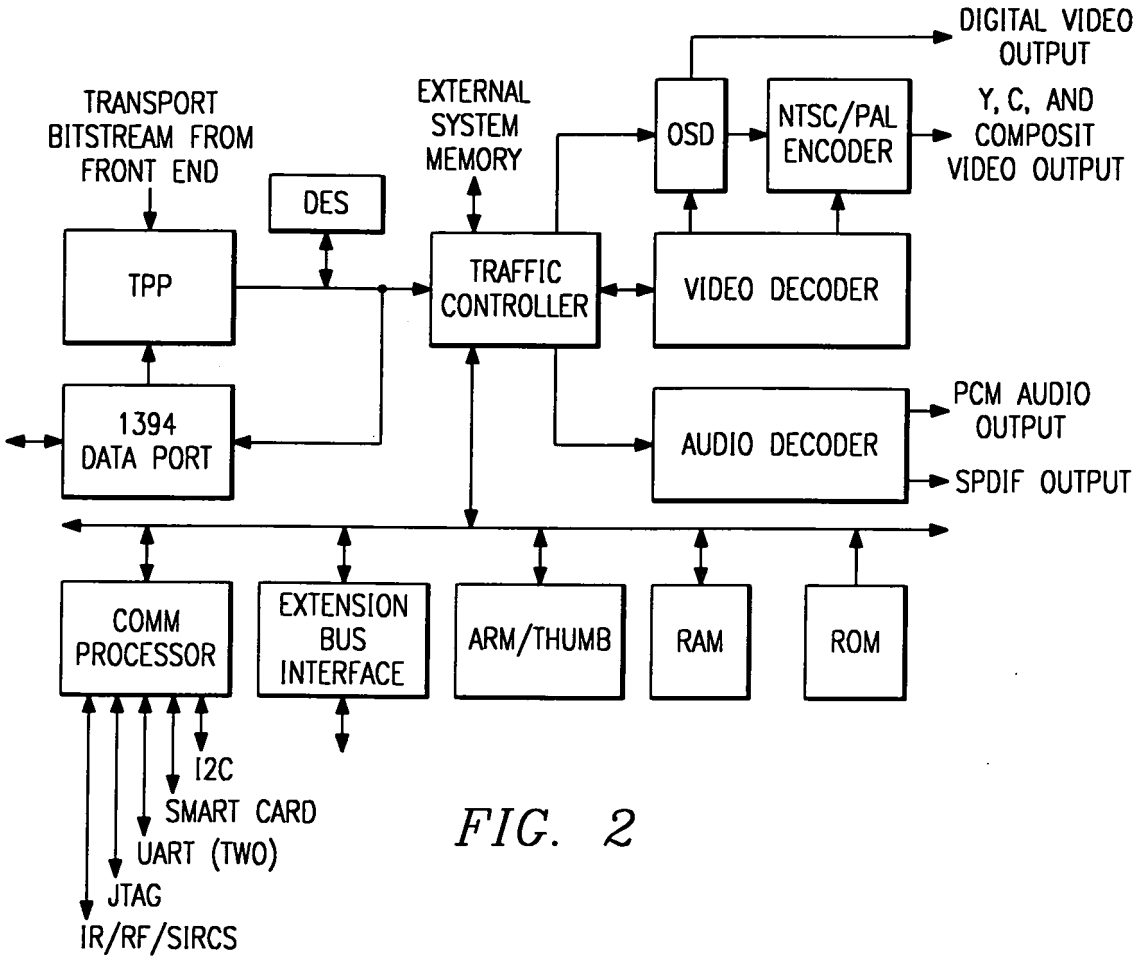

DIGITAL VIDEO OUTPUT
TRANSPORT BITSTREAM FROM FRONT END
EXTERNAL SYSTEM MEMORY
OSD
NTSC/PAL ENCODER
Y, C, AND COMPOSIT VIDEO OUTPUT
DES
TPP
TRAFFIC CONTROLLER
VIDEO DECODER
1394 DATA PORT
AUDIO DECODER
PCM AUDIO OUTPUT
SPDIF OUTPUT
COMM PROCESSOR
EXTENSION BUS INTERFACE
ARM/THUMB
RAM
ROM
I2C
SMART CARD
UART (TWO)
JTAG
IR/RF/SIRCS

FIG. 2

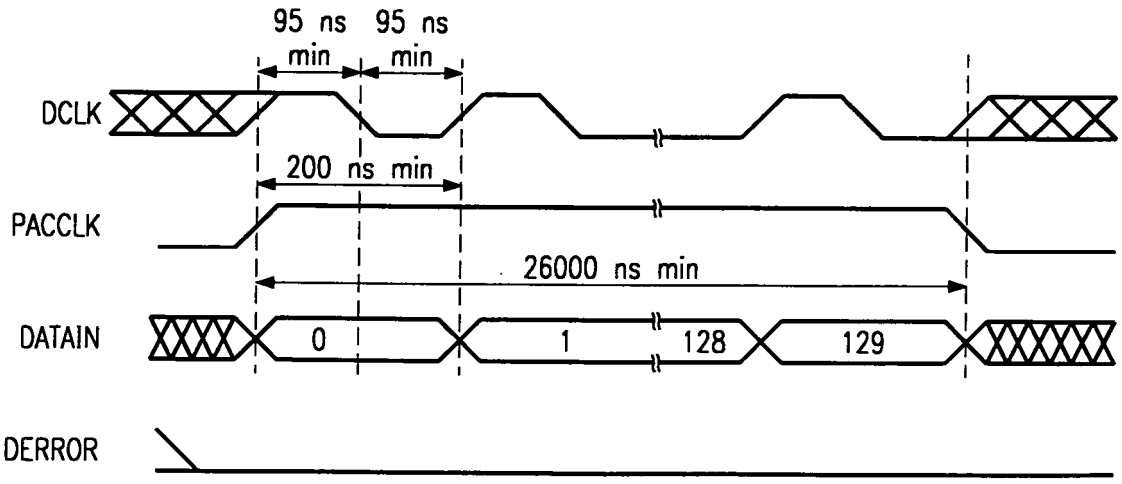

95 ns min
95 ns min
DCLK
200 ns min
PACCLK
26000 ns min
DATAIN
0
1
128
129
DERROR

FIG. 3

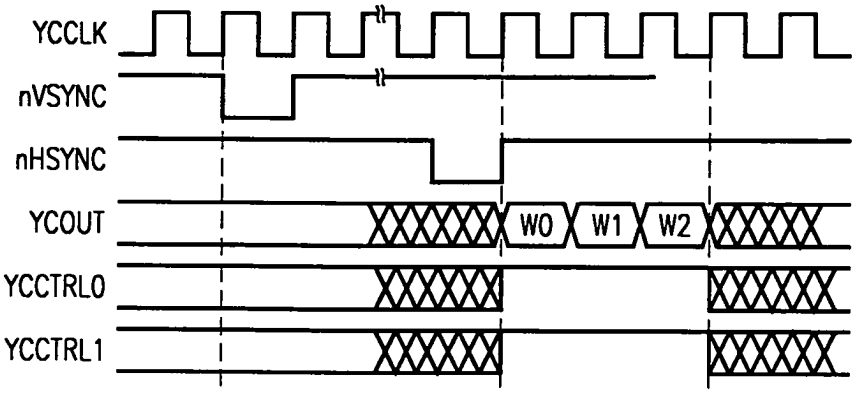


FIG. 4

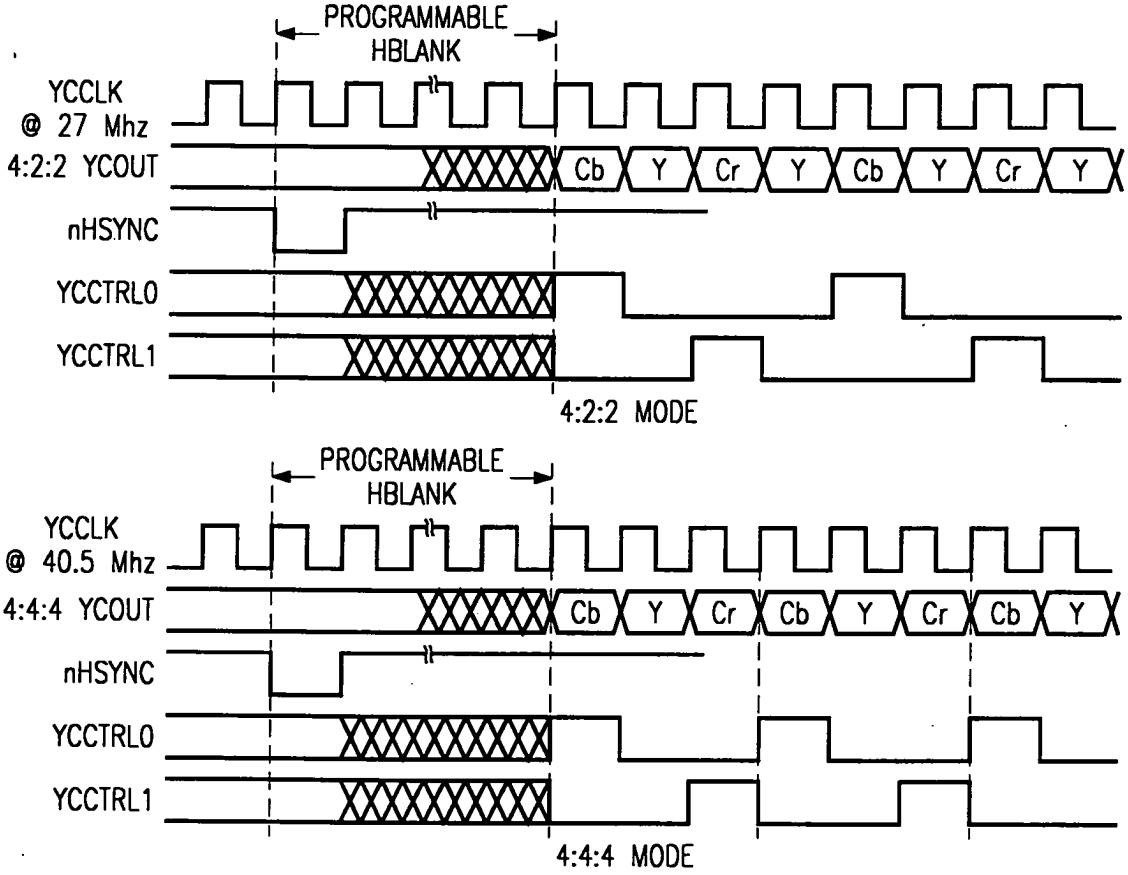


FIG. 5

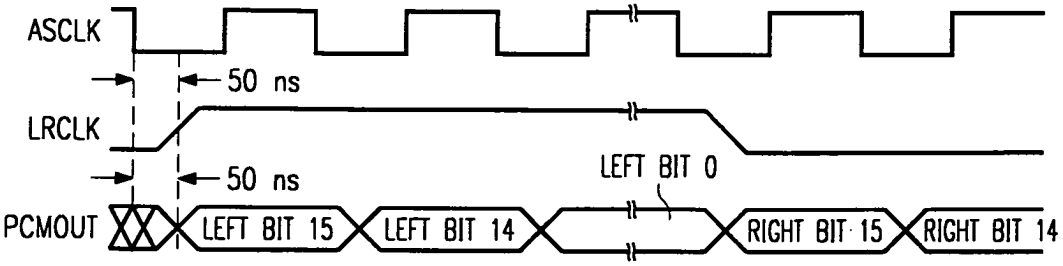


FIG. 6

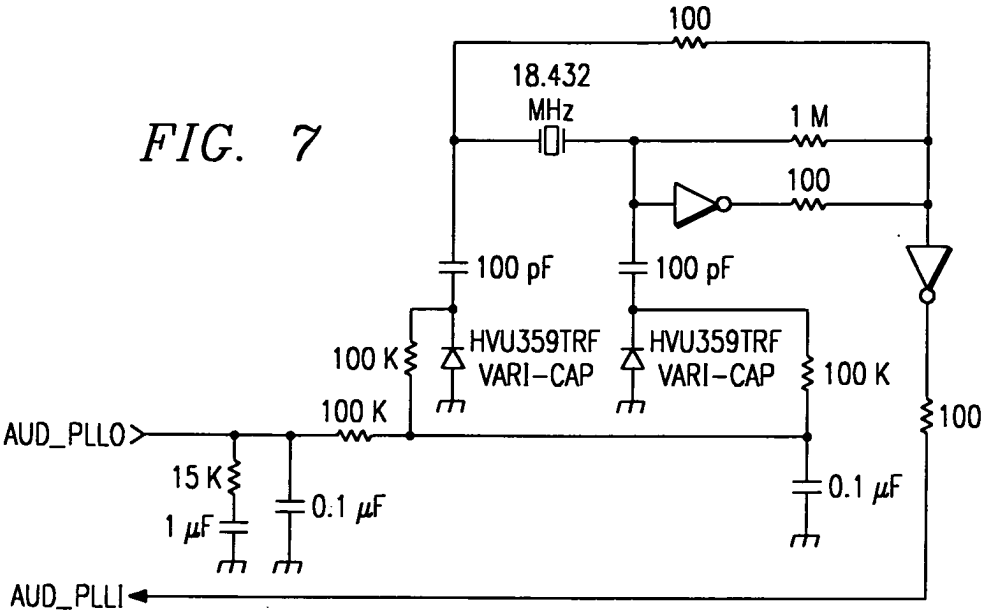


FIG. 7

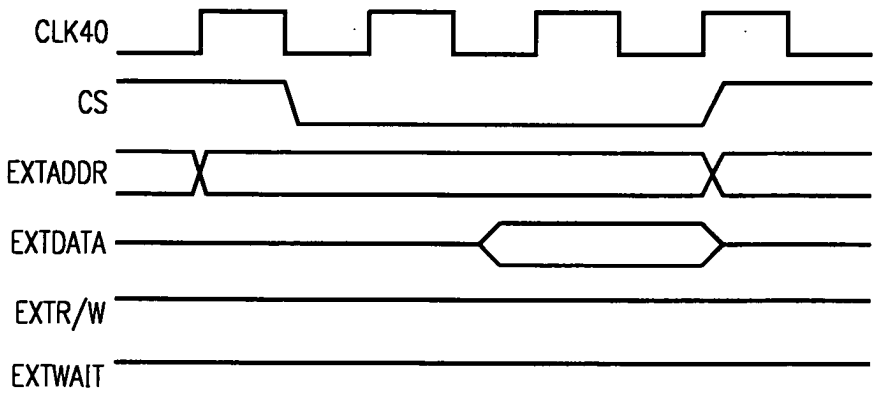


FIG. 8

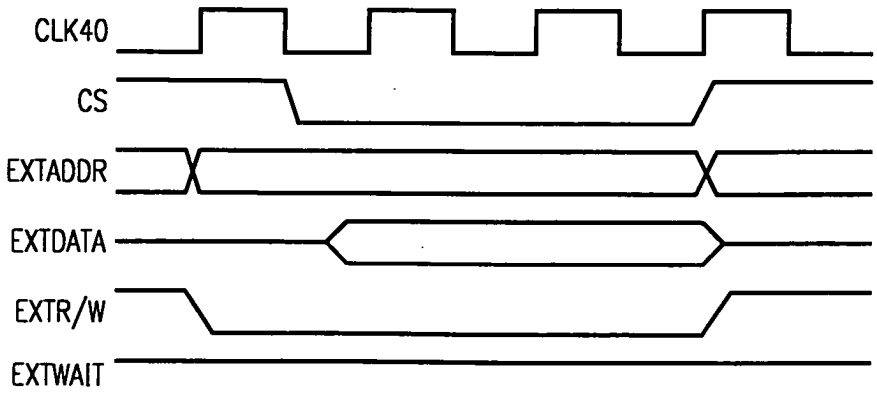


FIG. 9

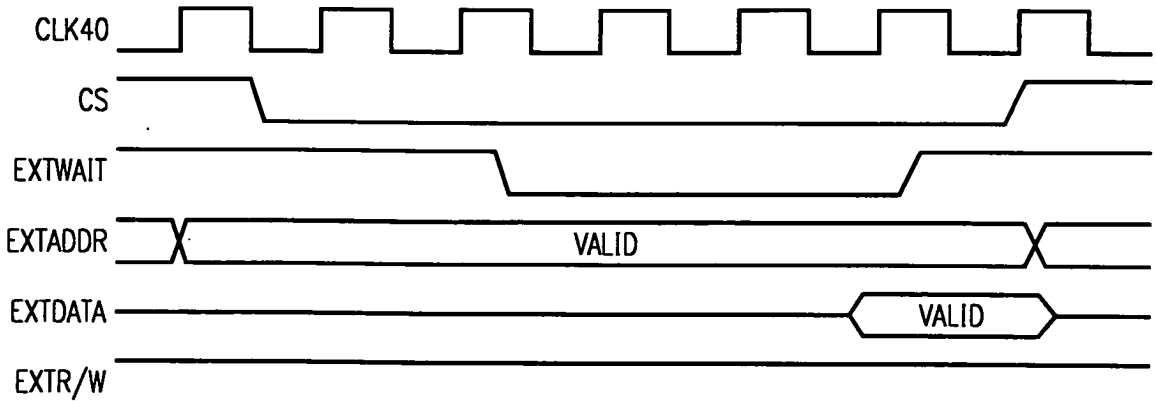


FIG. 10

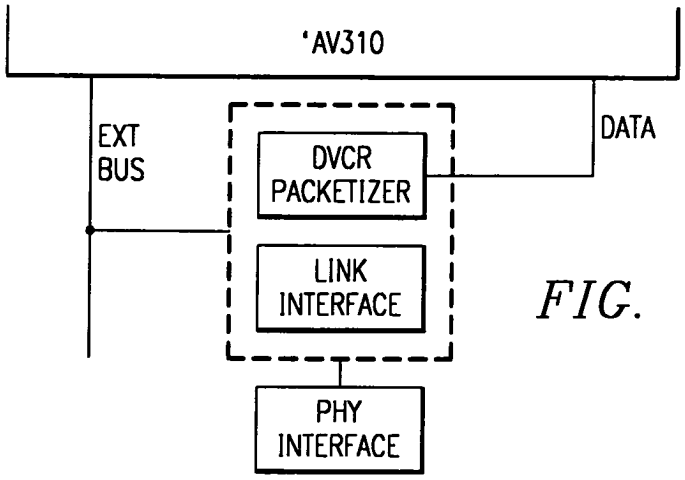


FIG. 11

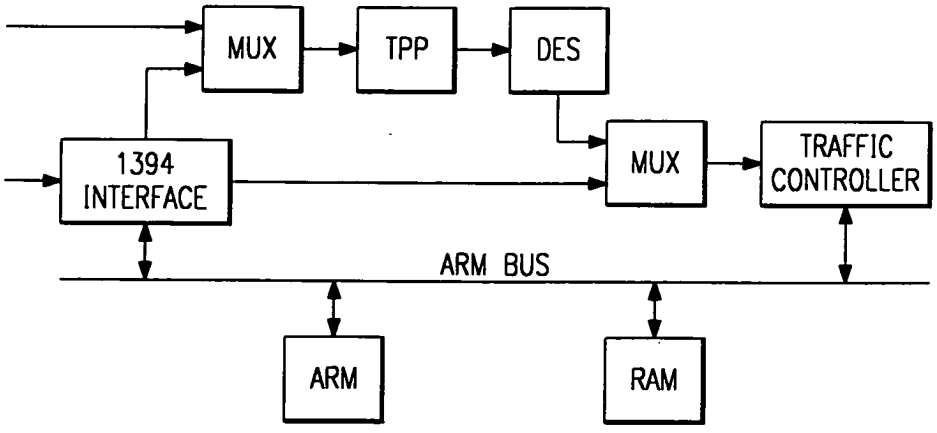


FIG. 12

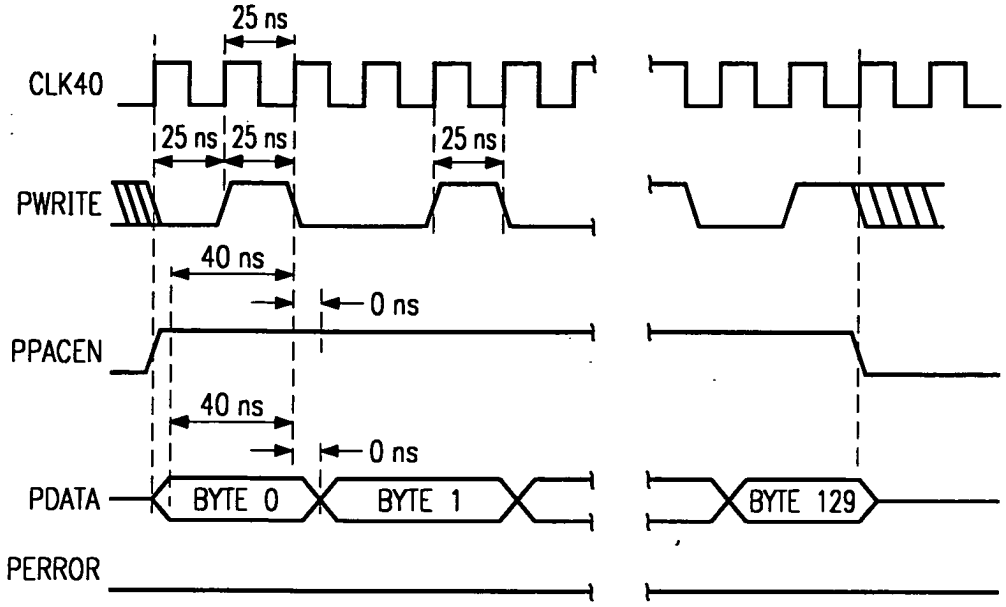

25 ns
CLK40
25 ns
25 ns
25 ns
PWRITE
40 ns
0 ns
PPACEN
40 ns
0 ns
PDATA
BYTE 0
BYTE 1
BYTE 129
PERROR

FIG. 13

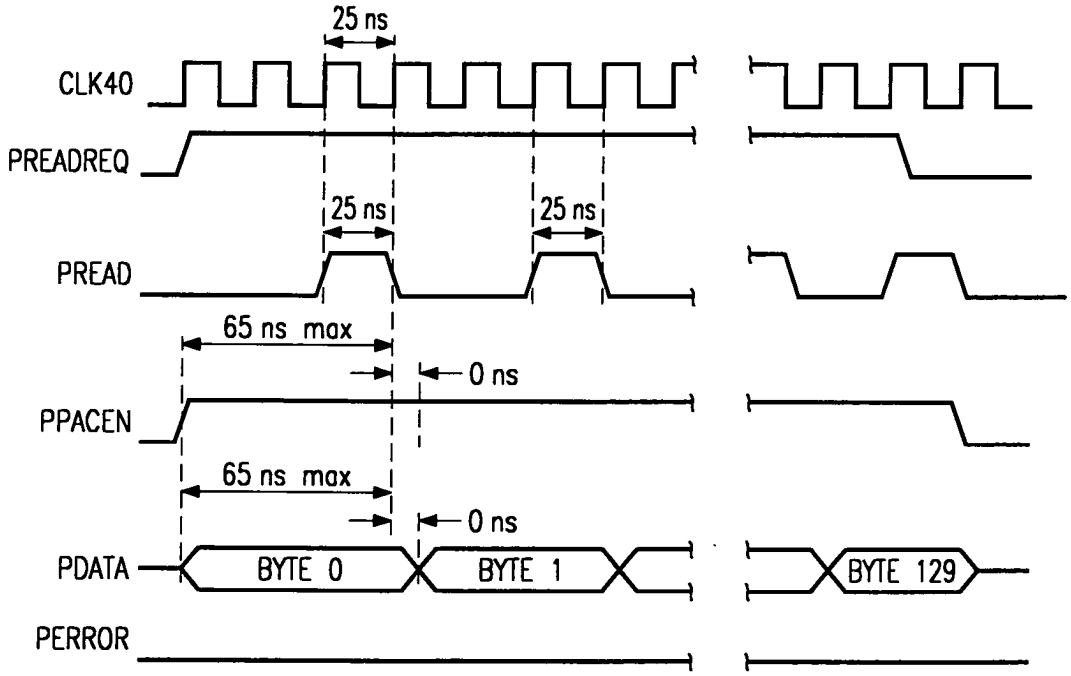

25 ns
CLK40
PREADREQ
25 ns
25 ns
PREAD
65 ns max
0 ns
PPACEN
65 ns max
0 ns
PDATA
BYTE 0
BYTE 1
BYTE 129
PERROR

FIG. 14

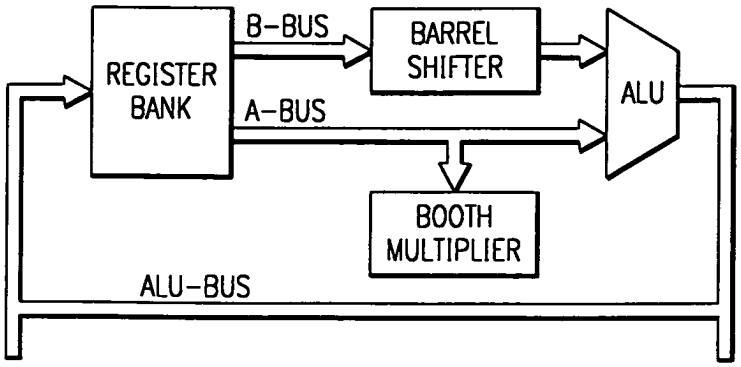

REGISTER BANK
B-BUS
BARREL SHIFTER
ALU
A-BUS
BOOTH MULTIPLIER
ALU-BUS

FIG. 15

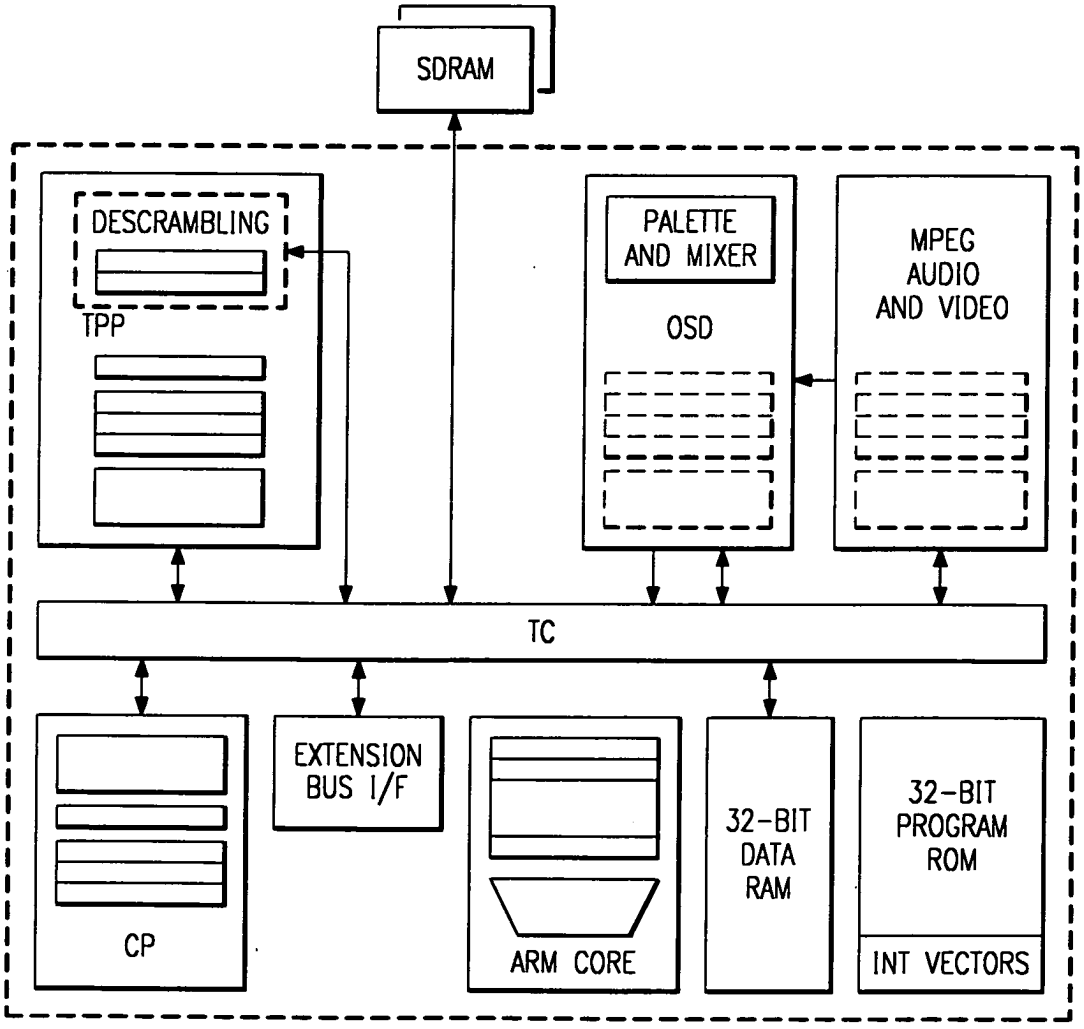

SDRAM
DESCRAMBLING
TPP
PALETTE AND MIXER
OSD
MPEG AUDIO AND VIDEO
TC
CP
EXTENSION BUS I/F
ARM CORE
32-BIT DATA RAM
32-BIT PROGRAM ROM
INT VECTORS

FIG. 16

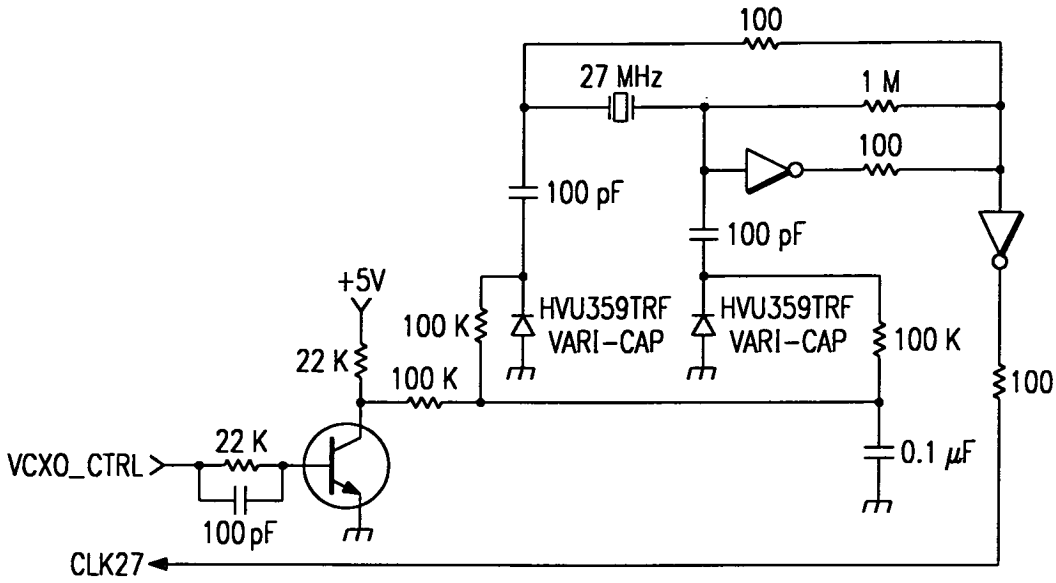

100
27 MHz
1 M
100
100 pF
100 pF
+5V
100 K
HVU359TRF
VARI-CAP
HVU359TRF
VARI-CAP
100 K
22 K
100 K
100
22 K
VCXO_CTRL
0.1 μF
100 pF
CLK27

FIG. 17

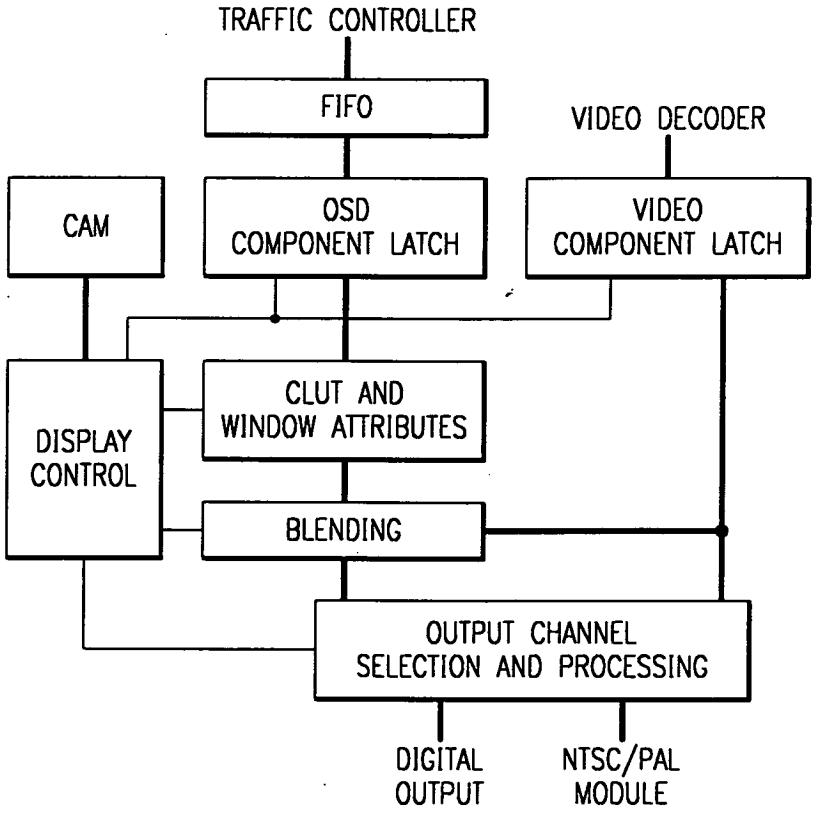

TRAFFIC CONTROLLER
FIFO
VIDEO DECODER
CAM
OSD
COMPONENT LATCH
VIDEO
COMPONENT LATCH
DISPLAY
CONTROL
CLUT AND
WINDOW ATTRIBUTES
BLENDING
OUTPUT CHANNEL
SELECTION AND PROCESSING
DIGITAL
OUTPUT
NTSC/PAL
MODULE

FIG. 18

CH2 DIGITAL VIDEO OUTPUT \ CH1 NTSC/PAL ENCODER OUTPUTS	VIDEO ONLY	FULL OSD PICTURE	NON-OVERLAPPED OSD	BOTTOM OF OVERLAPPED OSD
VIDEO ONLY	YES	YES	YES	YES
FULL OSD PICTURE	YES	YES	YES	NO
NON-OVERLAPPED OSD	YES	YES	YES	NO
TOP OF OVERLAPPED OSD	YES	YES	YES	NO

FIG. 19

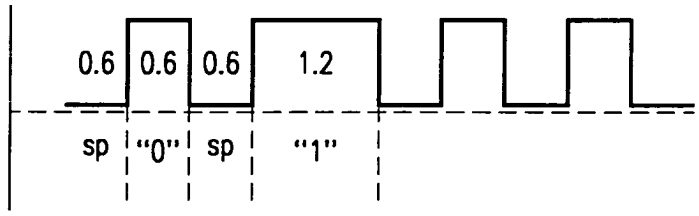


FIG. 20

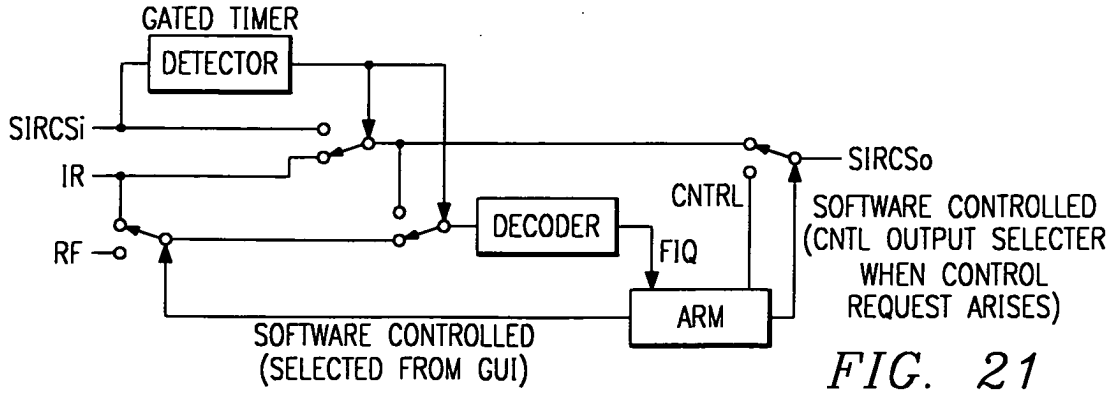


FIG. 21

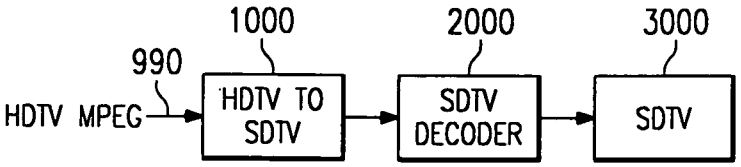


FIG. 22

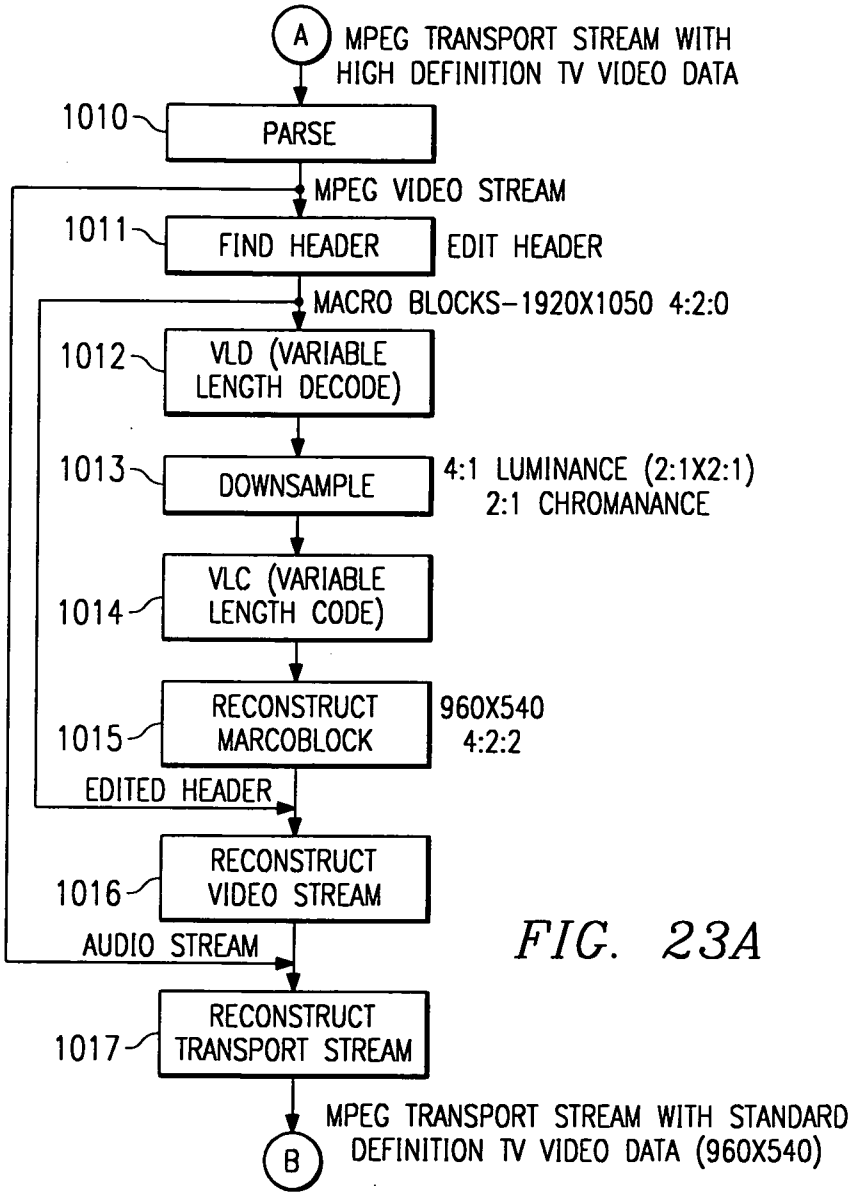


FIG. 23A

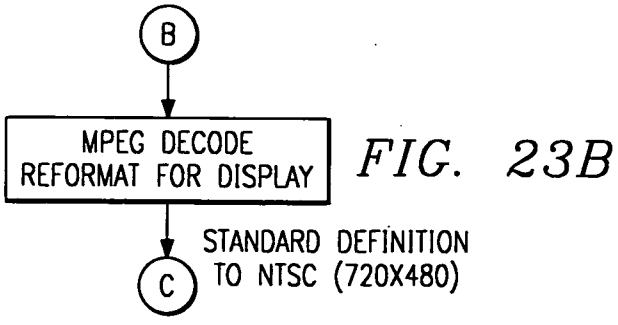


FIG. 23B

FIG. 24

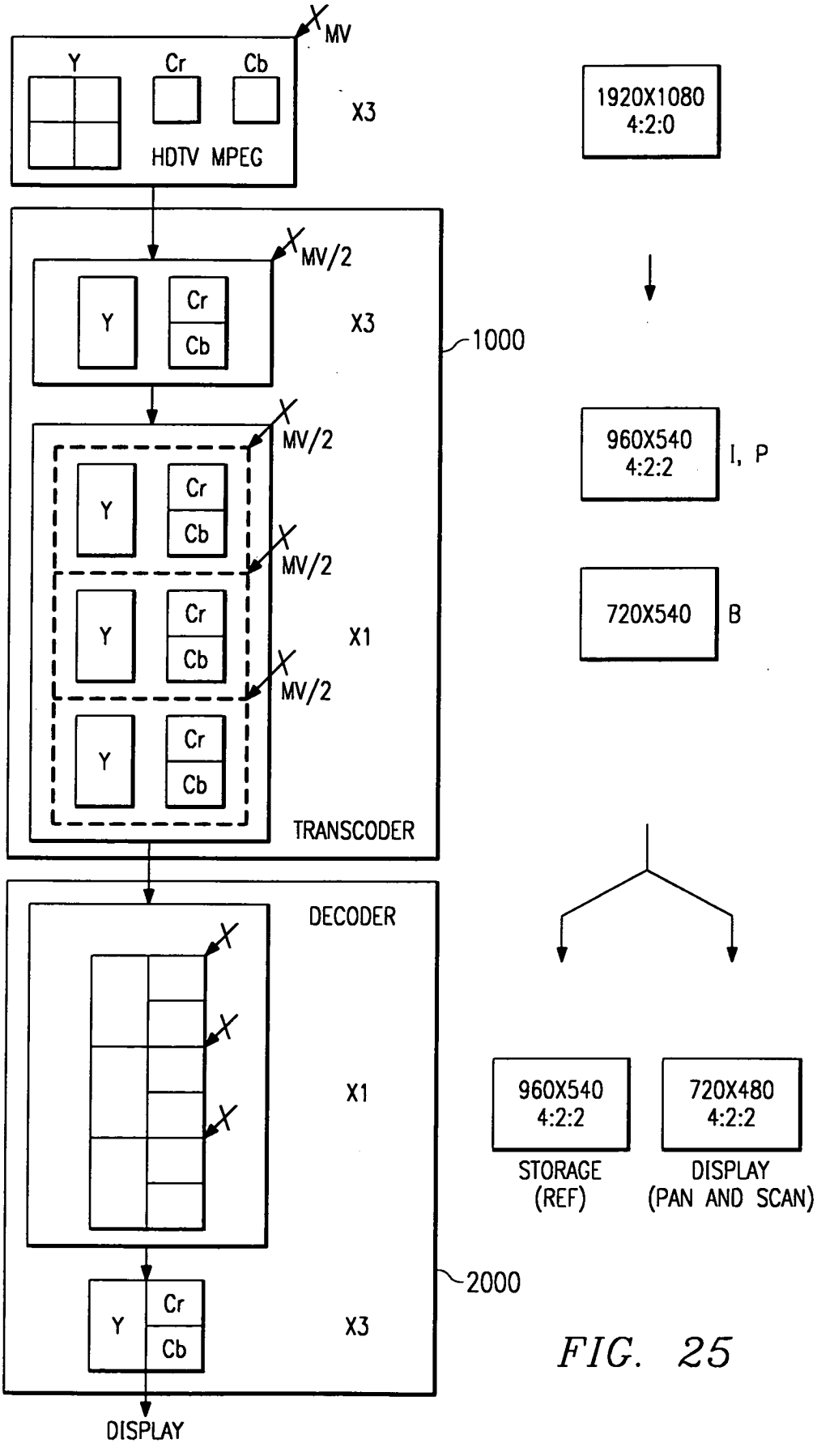

MV
Y
Cr
Cb
X3
HDTV MPEG
1920X1080
4:2:0
MV/2
X3
1000
960X540
4:2:2
I, P
X1
720X540
B
TRANSCODER
DECODER
960X540
4:2:2
720X480
4:2:2
STORAGE
(REF)
DISPLAY
(PAN AND SCAN)
2000
DISPLAY

FIG. 25

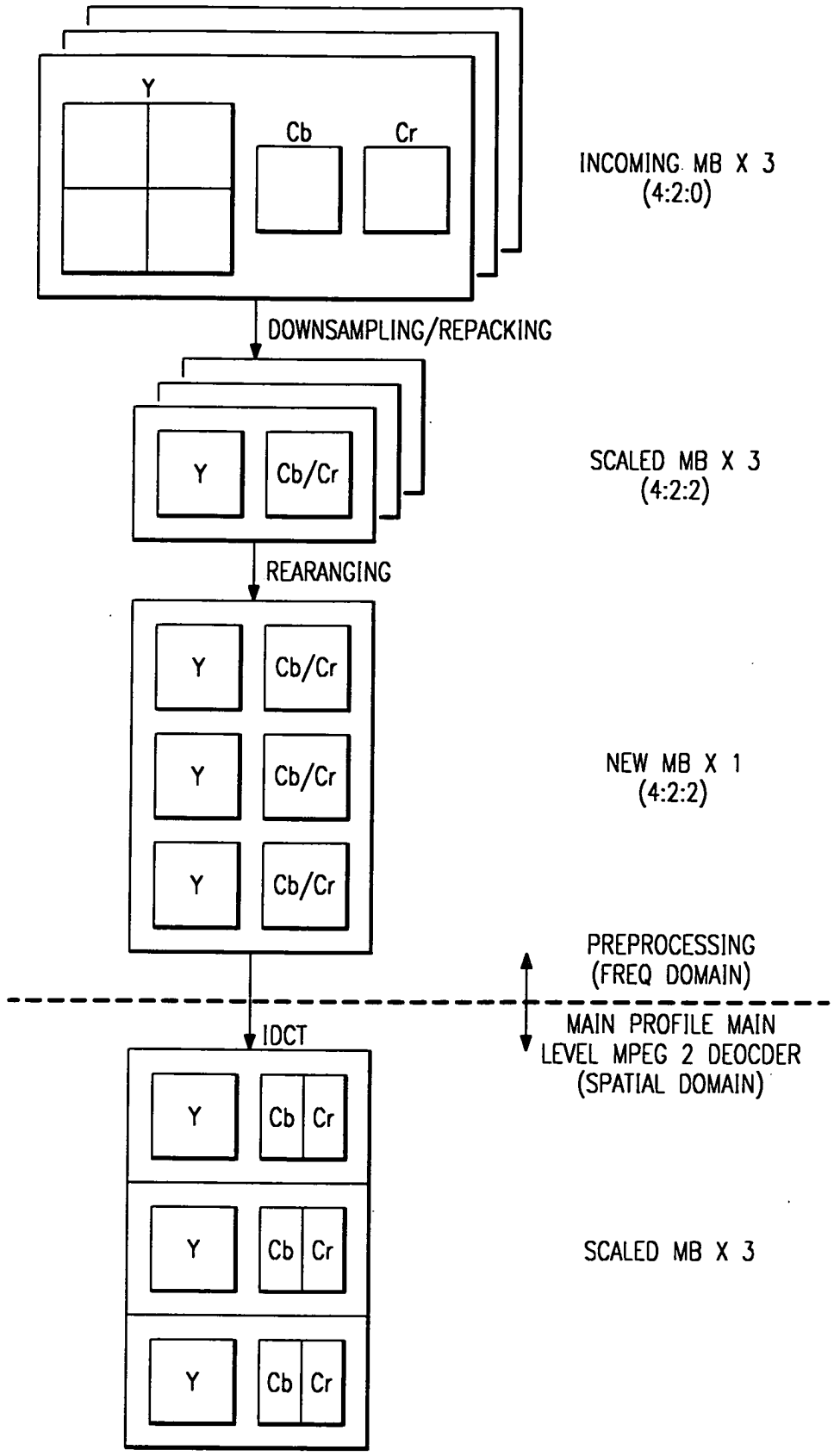

Y
Cb
Cr
INCOMING MB X 3
(4:2:0)
DOWNSAMPLING/REPACKING
Y
Cb/Cr
SCALED MB X 3
(4:2:2)
REARANGING
Y
Cb/Cr
Y
Cb/Cr
Y
Cb/Cr
NEW MB X 1
(4:2:2)
PREPROCESSING
(FREQ DOMAIN)
IDCT
MAIN PROFILE MAIN
LEVEL MPEG 2 DEOCDER
(SPATIAL DOMAIN)
Y
Cb
Cr
Y
Cb
Cr
Y
Cb
Cr
SCALED MB X 3

FIG. 26

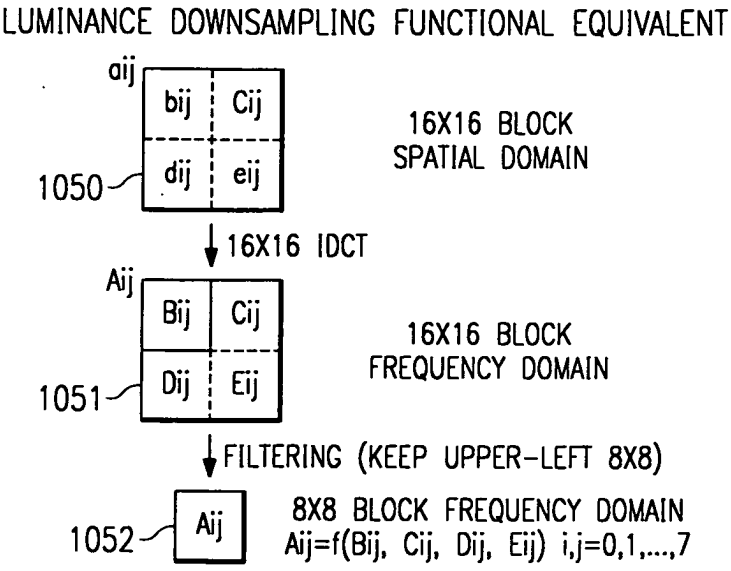


FIG. 27a

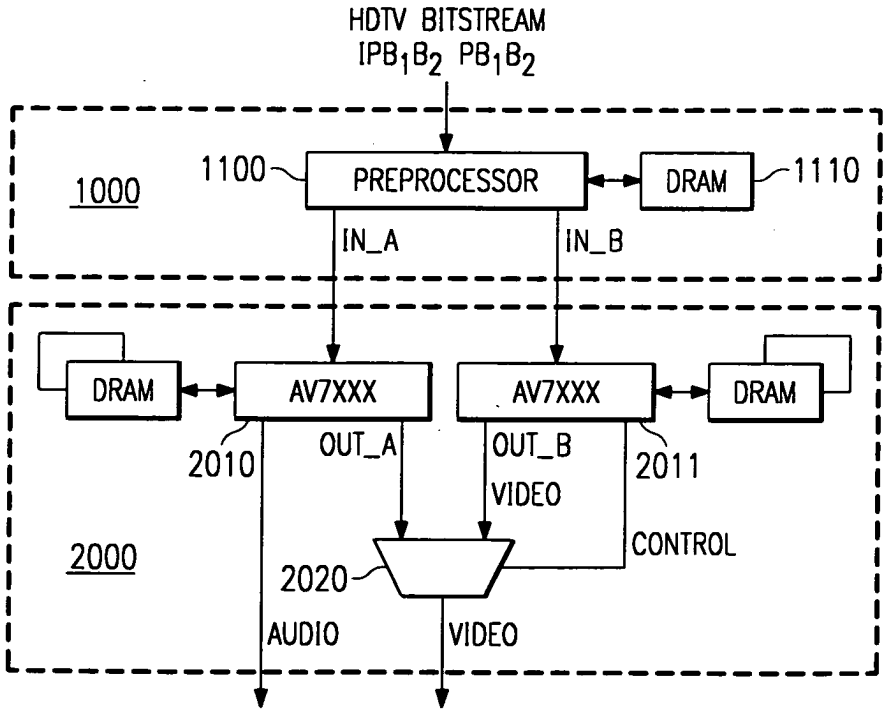
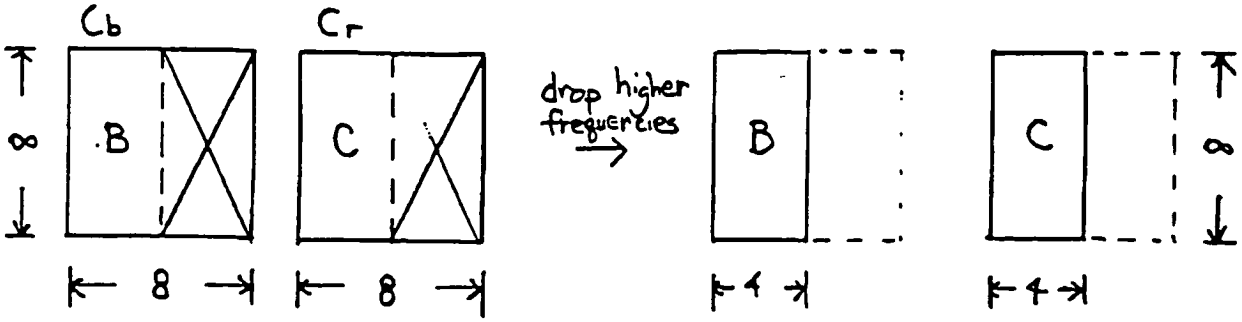


FIG. 28

⑤ Chrominance Down Sampling & Repacking

△ Downsampling (filtering):



△ Repacking:

Purpose of repacking is to prepare data in such a way that a 8×8 IDCT would recover b & c directly.

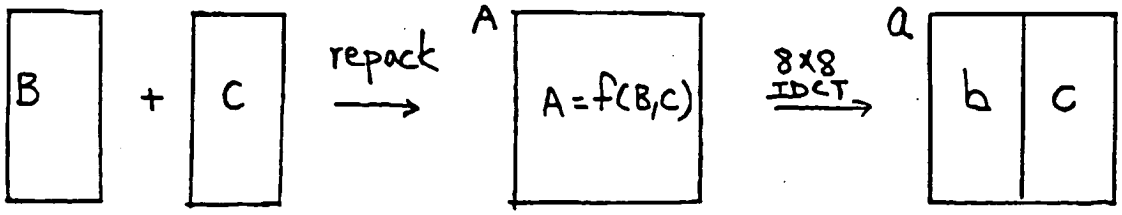


Fig. 27b

FUNCTIONAL BLOCK DIAGRAM OF THE TRANSCODER CHIP

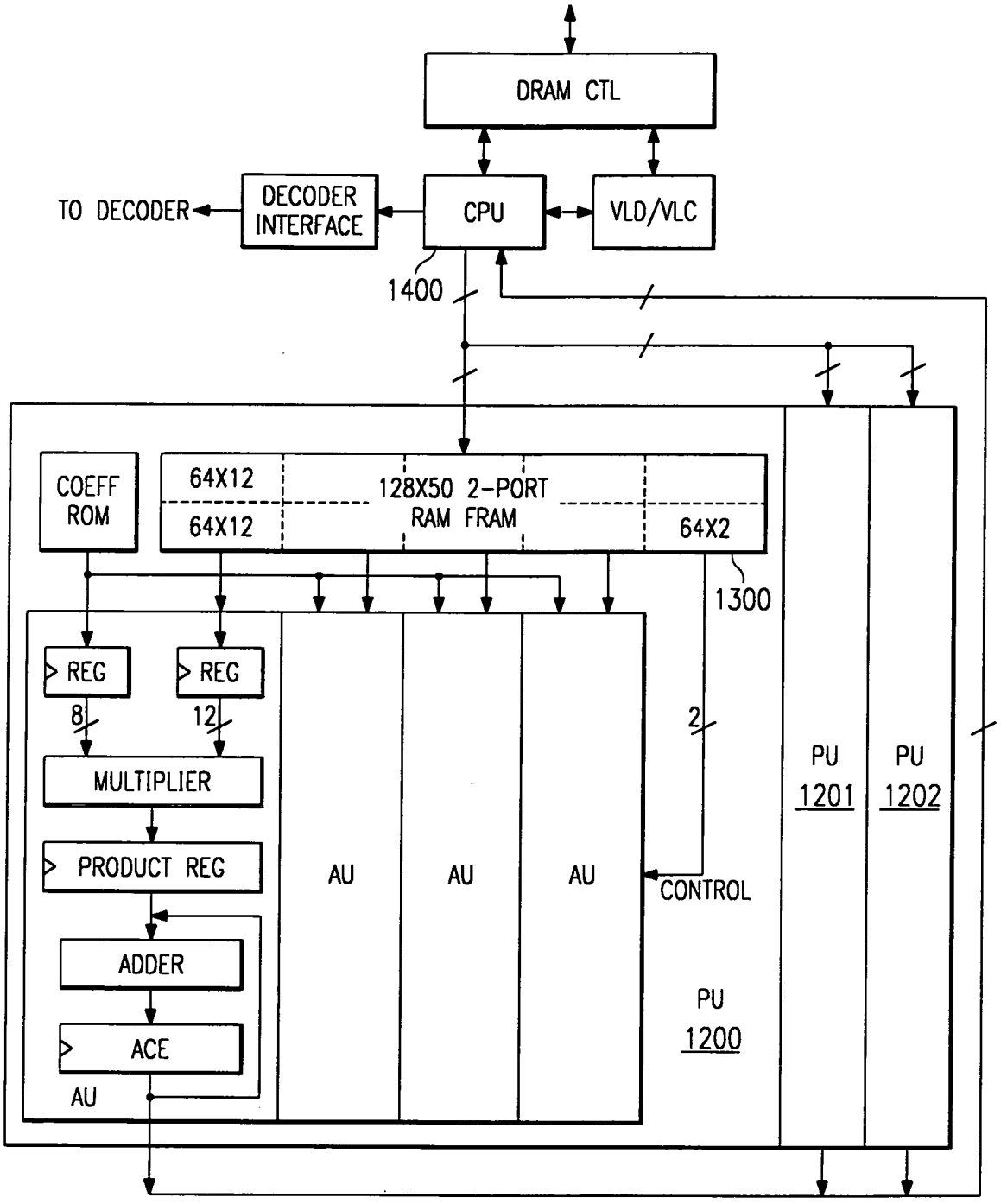
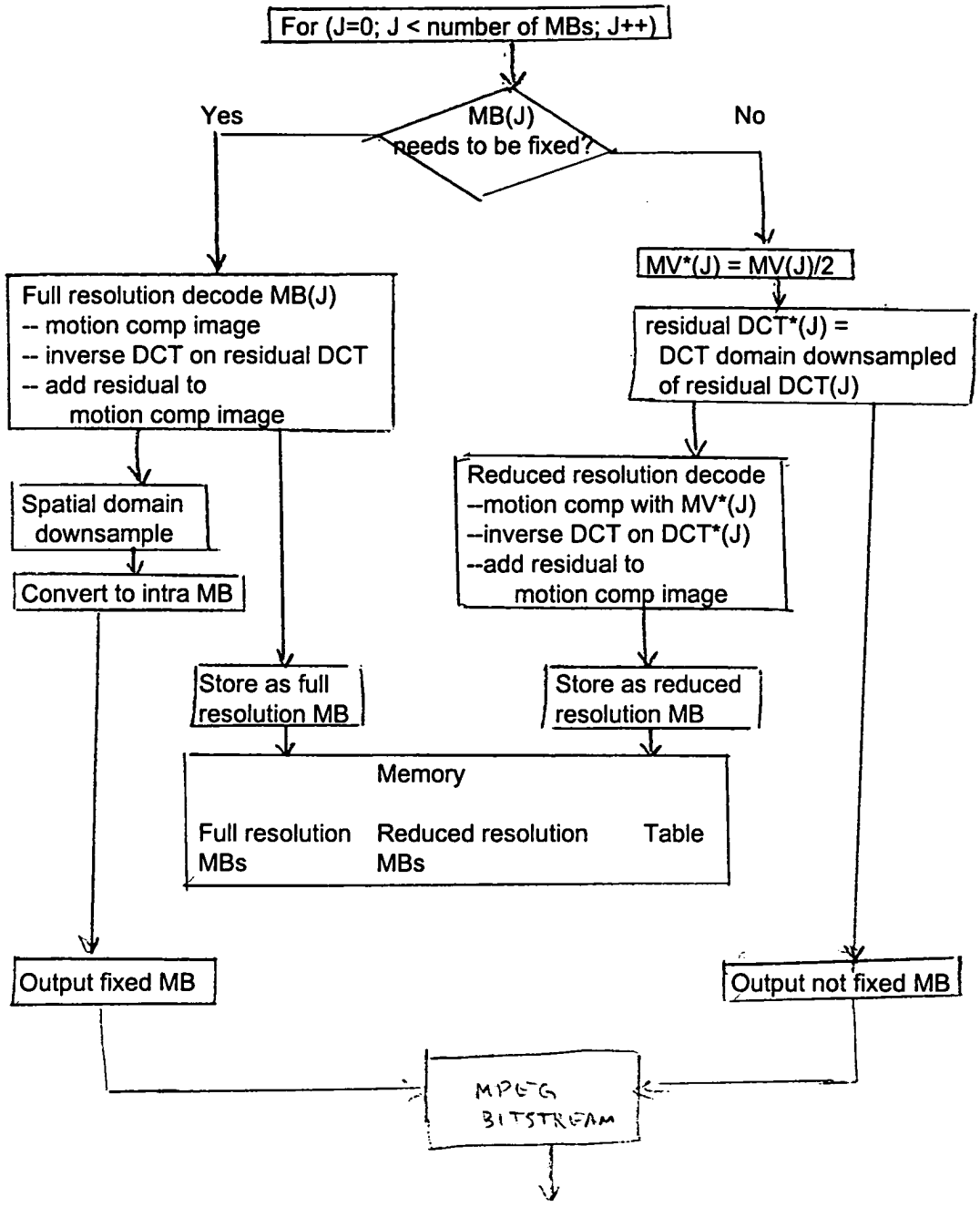


FIG. 29



AV7xx, AV3xx

Fig. 30a

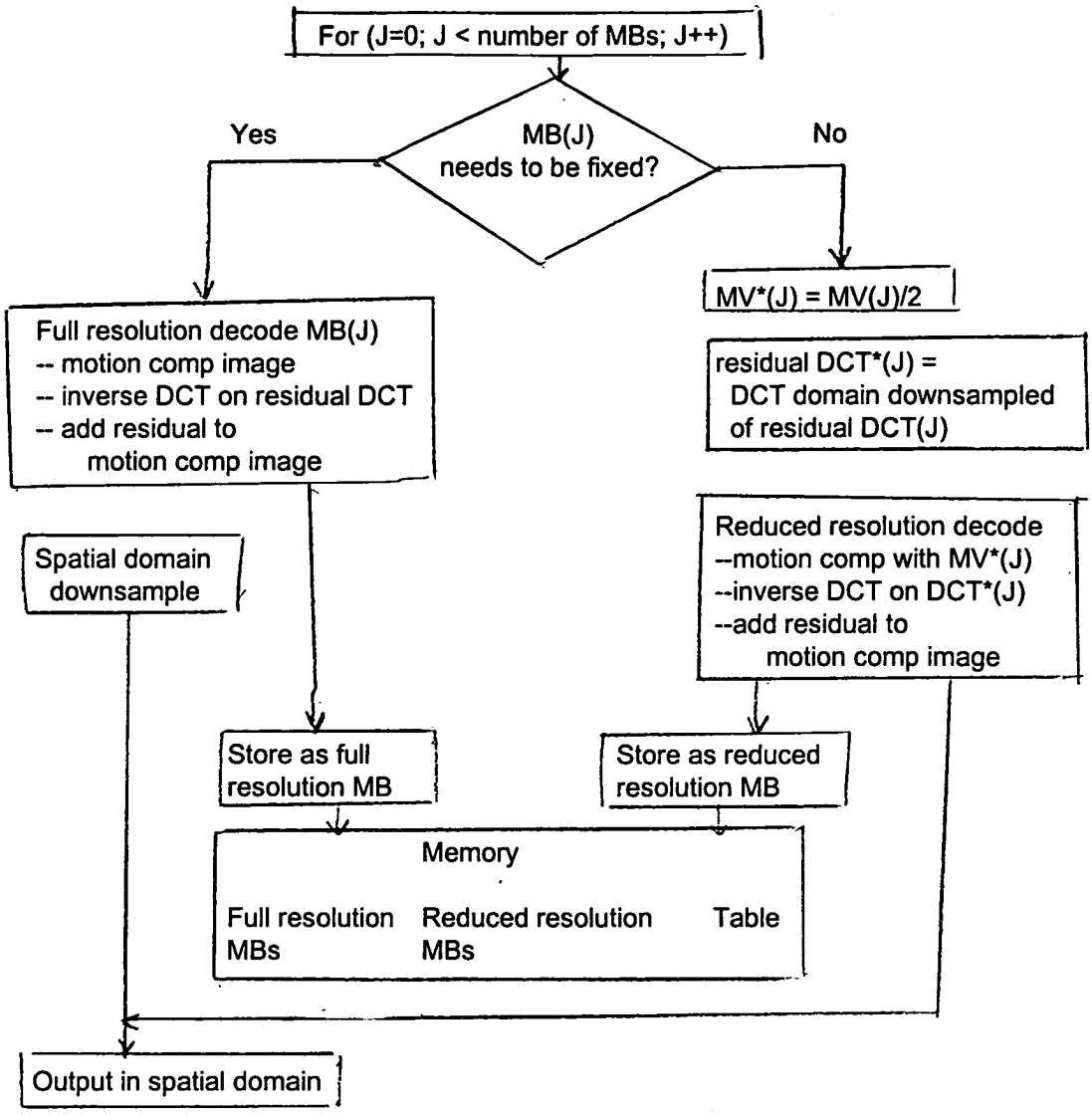

For (J=0; J < number of MBs; J++)
MB(J) needs to be fixed?
Yes
No
Full resolution decode MB(J)
-- motion comp image
-- inverse DCT on residual DCT
-- add residual to motion comp image
MV*(J) = MV(J)/2
residual DCT*(J) = DCT domain downsampled of residual DCT(J)
Spatial domain downsample
Reduced resolution decode
--motion comp with MV*(J)
--inverse DCT on DCT*(J)
--add residual to motion comp image
Store as full resolution MB
Store as reduced resolution MB
Memory
Full resolution MBs
Reduced resolution MBs
Table
Output in spatial domain

Fig. 30b

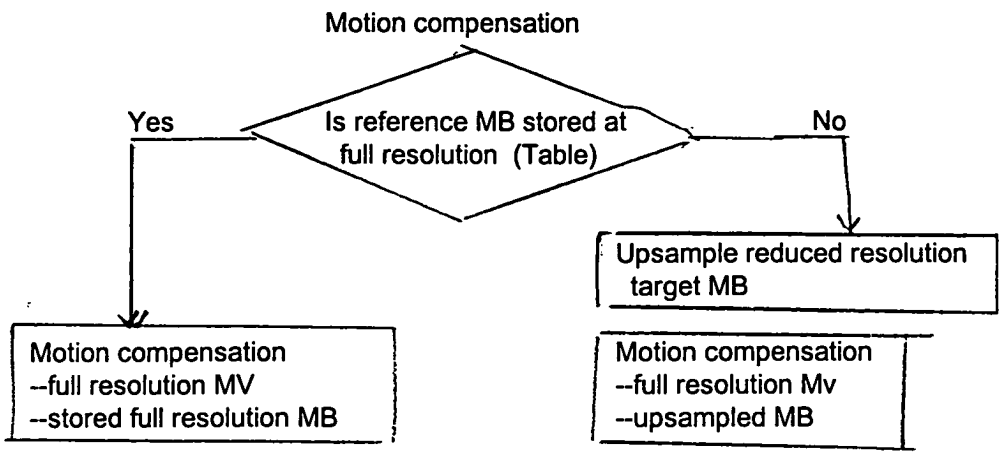

Motion compensation
Is reference MB stored at full resolution (Table)
Yes
No
Upsample reduced resolution target MB
Motion compensation
--full resolution MV
--stored full resolution MB
Motion compensation
--full resolution Mv
--upsampled MB

Fig. 30c

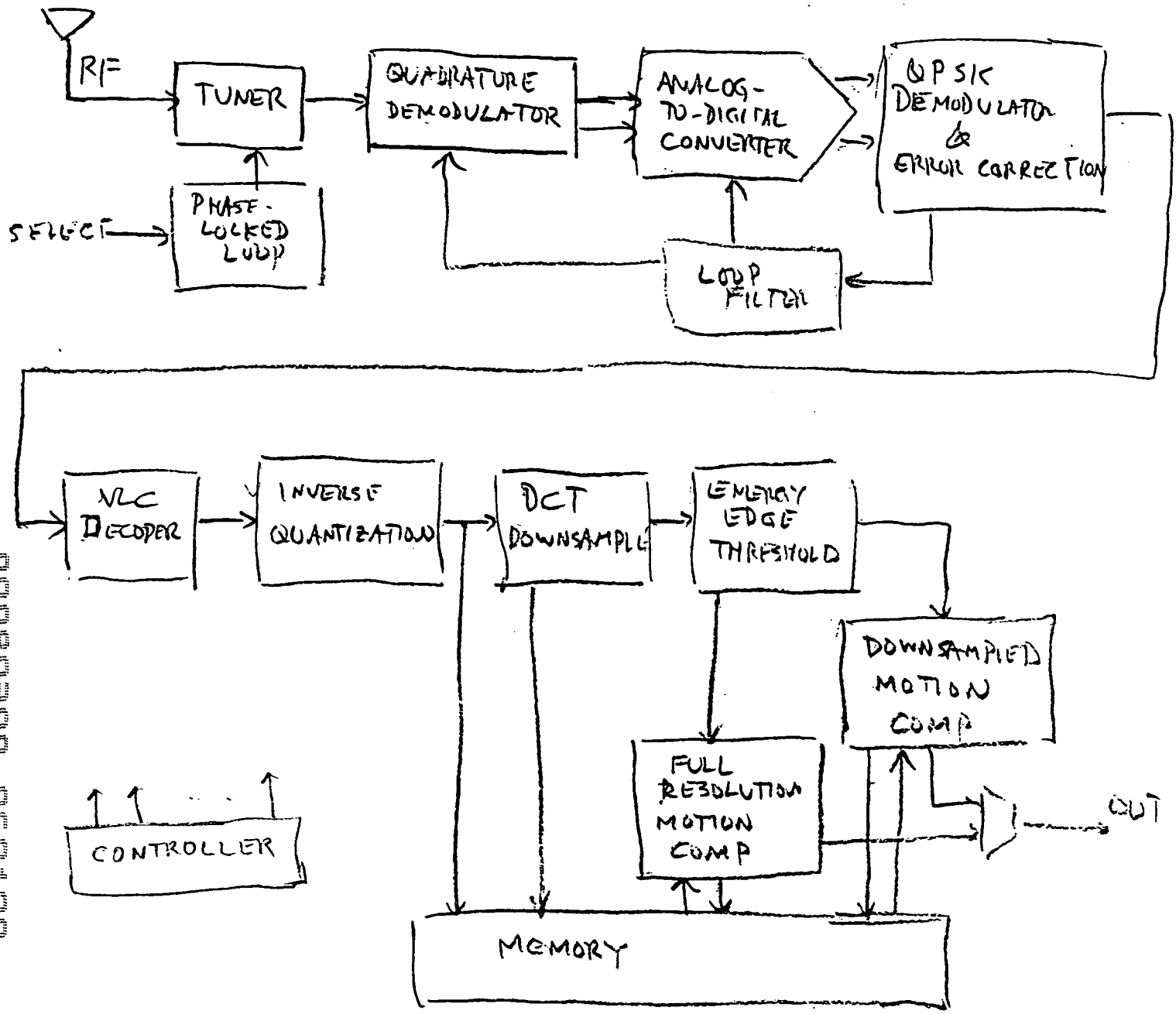

RF
TUNER
QUADRATURE DEMODULATOR
ANALOG-TO-DIGITAL CONVERTER
QPSK DEMODULATOR & ERROR CORRECTION
SELECT
PHASE-LOCKED LOOP
LOOP FILTER
VLC DECODER
INVERSE QUANTIZATION
DCT
EMERGY EDGE THRESHOLD
DOWNSAMPLED MOTION COMP
FULL RESOLUTION MOTION COMP
OUT
CONTROLLER
MEMORY

Fig. 31

Generic Data Flow of Transcoder

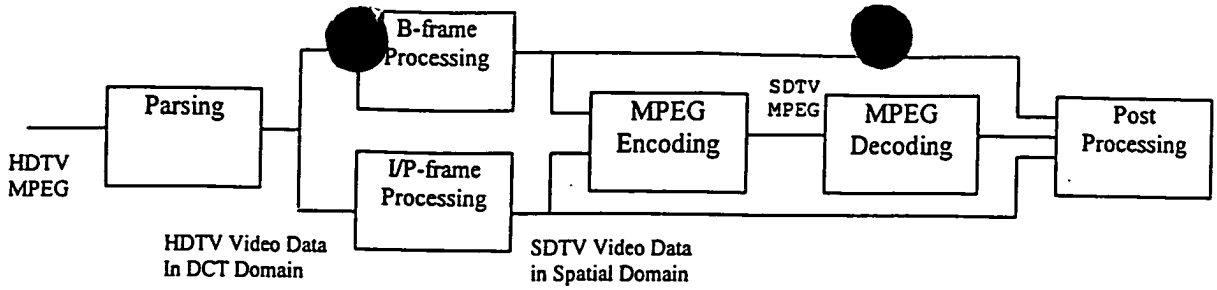


Fig 32a

Transcoder Option 1: utilizing existing SDTV MPEG decoder

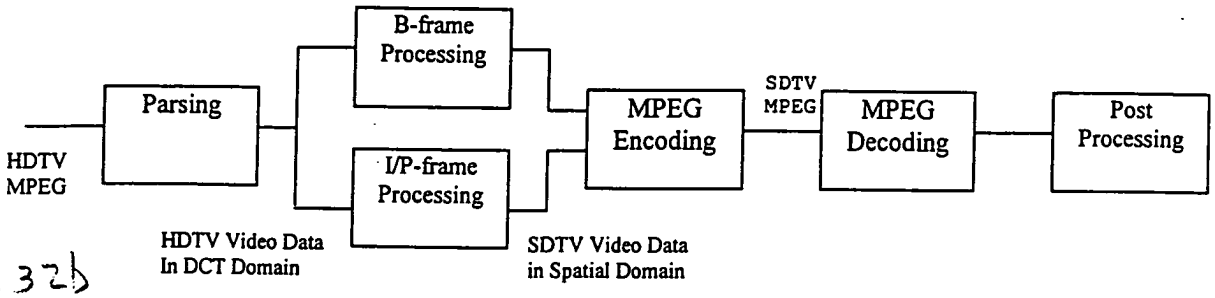


Fig. 32b

Transcoder Option 2: direct decoding

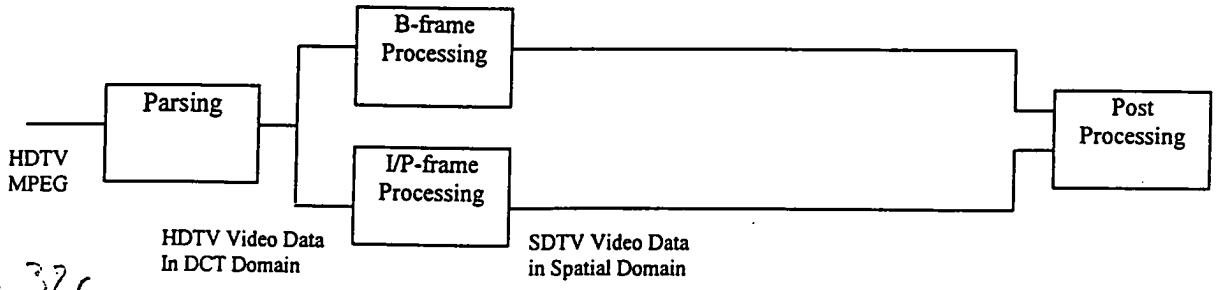


Fig. 32c

Transcoder Option 3: combination of options 1 and 2

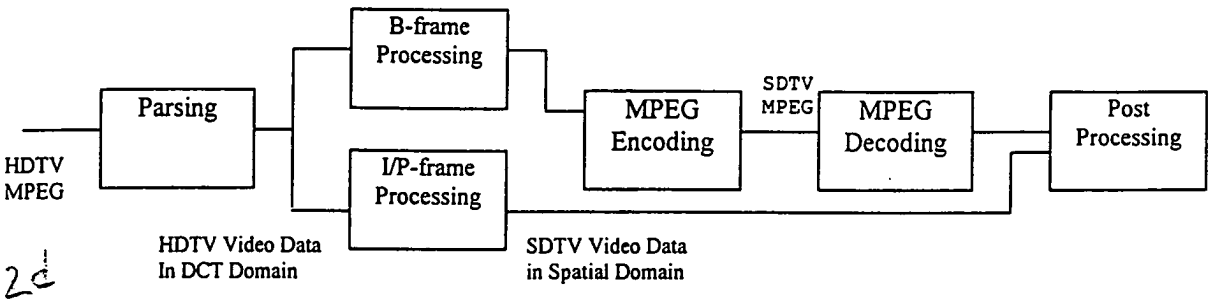


Fig. 32d

~~**B Frame Processing**~~

~~Perform downsampling operation as described in Part I, HDTV downsampling Operation, followed by~~ motion compensation.

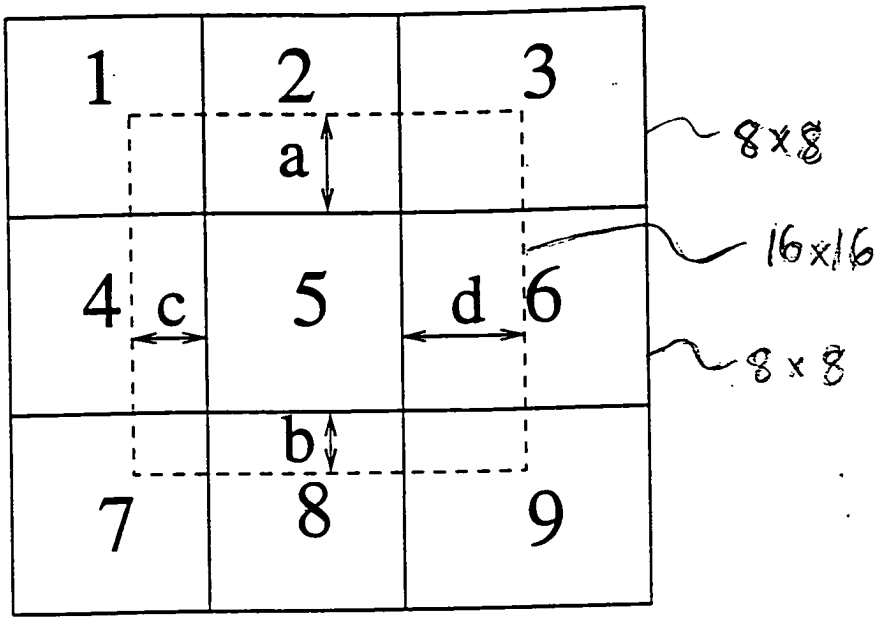


Fig. 33